HEWLETT-PACKARD COMPANY
Intellectual Property Administration
P.O. Box 272400
Fort Collins, Colorado 80527-2400

PATENT APPLICATION

ATTORNEY DOCKET NO. 200308581-1

IN THE
UNITED STATES PATENT AND TRADEMARK OFFICE

Inventor(s): Andrew H. Barr et al.

Confirmation No.: 3950

Application No.: 10/714,386

Examiner: Aditya S. Bhat

Filing Date: Nov. 14, 2003

Group Art Unit: 2863

Title: SYSTEM AND METHOD FOR TESTING A MEMORY WITH AN EXPANSION CARD USING DMA

Mail Stop Appeal Brief-Patents
Commissioner For Patents
PO Box 1450
Alexandria, VA 22313-1450

TRANSMITTAL OF APPEAL BRIEF

Transmitted herewith is the Appeal Brief in this application with respect to the Notice of Appeal filed on Sep. 13, 2006.

The fee for filing this Appeal Brief is (37 CFR 1.17(c)) $500.00.

(complete (a) or (b) as applicable)

The proceedings herein are for a patent application and the provisions of 37 CFR 1.136(a) apply.

☐ (a) Applicant petitions for an extension of time under 37 CFR 1.136 (fees: 37 CFR 1.17(a)-(d)) for the total number of months checked below:

☐ 1st Month $120	☐ 2nd Month $450	☐ 3rd Month $1020	☐ 4th Month $1590

☐ The extension fee has already been filed in this application.

☒ (b) Applicant believes that no extension of time is required. However, this conditional petition is being made to provide for the possibility that applicant has inadvertently overlooked the need for a petition and fee for extension of time.

Please charge to Deposit Account 08-2025 the sum of $ 500. At any time during the pendency of this application, please charge any fees required or credit any over payment to Deposit Account 08-2025 pursuant to 37 CFR 1.25. Additionally please charge any fees to Deposit Account 08-2025 under 37 CFR 1.16 through 1.21 inclusive, and any other sections in Title 37 of the Code of Federal Regulations that may regulate fees. A duplicate copy of this sheet is enclosed.

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Respectfully submitted,
Andrew H. Barr et al.
By_____
Christopher P. Kosh
Attorney/Agent for Applicant(s)
Reg No. : 42,760
Date : Nov. 13, 2006
Telephone : (512) 241-2403

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Applicant:	Andrew H. Barr et al.	Examiner: Aditya S. Bhat
Serial No.:	10/714,386	Group Art Unit: 2863
Filed:	Nov. 14, 2003	Docket: 200308581-1
Due Date:	Nov. 13, 2006	
Title:	SYSTEM AND METHOD FOR TESTING A MEMORY WITH AN EXPANSION CARD USING DMA	

APPEAL BRIEF UNDER 37 C.F.R. § 41.37

Mail Stop Appeal Brief – Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir/Madam:

This Appeal Brief is submitted in support of the Notice of Appeal filed on September 13, 2006, appealing the final rejection of claims 1-20 of the above-identified application as set forth in the Final Office Action mailed May 18, 2006.

The U.S. Patent and Trademark Office is hereby authorized to charge Deposit Account No. 08-2025 in the amount of $500.00 for filing a Brief in Support of an Appeal as set forth under 37 C.F.R. § 41.20(b)(2). At any time during the pendency of this application, please charge any required fees or credit any overpayment to Deposit Account No. 08-2025.

Appellant respectfully requests consideration and reversal of the Examiner's rejection of pending claims 1-20.

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REAL PARTY IN INTEREST

The real party in interest is HEWLETT-PACKARD DEVELOPMENT COMPANY, L.P..

RELATED APPEALS AND INTERFERENCES

There are no other appeals or interferences known to Appellant that will have a bearing on the Board's decision in the present Appeal.

STATUS OF CLAIMS

In a Final Office Action mailed May 18, 2006, claims 1-20 were rejected. Claims 1-20 are pending in the application. Claims 1-20 are the subject of the present Appeal.

STATUS OF AMENDMENTS

No amendments have been entered subsequent to the Final Office Action mailed May 18, 2006.

SUMMARY OF THE CLAIMED SUBJECT MATTER

One aspect of the present invention, as claimed in independent claim 1, provides a computer system (100) with a test module card (150). The computer system includes a processor (110) configured to execute an operating system, a memory controller (122 or 428), a memory (130), an input/output (I/O) controller (124 or 424), an expansion slot, and a test module card (150) directly coupled to the expansion slot. *See, e.g.,* Specification page 3, lines 12-22 and page 8, lines 11-26 and Figures 1 and 4. The test module card is configured to obtain access to a portion (202) of the memory from the operating system and cause tests to be performed on the portion of the memory using direct memory access (DMA) subsequent to obtaining access to the portion of the memory. *See, e.g.,* Specification, page 3, lines 3-11; page 5, lines 1-15; and page 6, line 9 to page 7, line 10 and Figures 2 and 3.

One aspect of the present invention, as claimed in independent claim 9, provides a method of testing a memory (130) of a computer system (100). The method includes obtaining access to a portion (202) of a memory (130) of a computer system (100) from an operating system during operation of a computer system, generating a test transaction in a test module card (150) directly coupled to an expansion slot of the computer system, and providing the test transaction to the portion using direct memory access (DMA) subsequent to obtaining access to the portion of the memory. *See, e.g.,* Specification, page 3, lines 3-11; page 5, lines 1-15; and page 6, line 9 to page 7, line 10 and Figures 2 and 3.

One aspect of the present invention, as claimed in independent claim 15, provides a computer system (100) with a test module card (150). The computer system includes a processor (110), a memory controller (122 or 428) configured to perform error correction, a memory (130), an input/output (I/O) controller (124 or 424), an expansion slot, and a test module card (150) directly coupled to the expansion slot. *See, e.g.,* Specification page 3, lines 12-22 and page 8, lines 11-26 and Figures 1 and 4. The test module card is configured to obtain access to a portion (202) of the memory from the operating system and cause tests to be performed on the portion of the memory by providing read transactions associated with the memory to the I/O controller subsequent to obtaining access to the portion of the memory. *See, e.g.,* Specification, page 3, lines 3-11; page 5, lines 1-15; and page 6, line 9 to page 7, line 10 and Figures 2 and 3.

GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

Claims 1-20 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Jenkins et al. U.S. Patent No. 6,002,868 ("Jenkins") in view of Brickman et al. U.S. Patent No. 4,315,330 ("Brickman").

ARGUMENT

I. The Applicable Law

The Examiner has the burden under 35 U.S.C. §103 to establish a *prima facie* case of obviousness. *In re Fine,* 837 F.2d 1071, 1074, 5 USPQ2d 1596, 1598 (Fed. Cir. 1988). Three criteria must be satisfied to establish a *prima facie* case of obviousness. First, the Examiner must show that some objective teaching in the prior art or some knowledge generally available to one of ordinary skill in the art would teach, suggest, or motivate one to modify a reference or to combine the teachings of multiple references. *Id.* Second, the prior art can be modified or combined only so long as there is a reasonable expectation of success. *In re Merck & Co., Inc.,* 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986). Third, the prior art reference or combined prior art references must teach or suggest all of the claim limitations. *In re Royka,* 490 F.2d 981, 180 USPQ 580 (CCPA 1974). These three criteria are also set forth in §§706.02(j) and 2143 of the M.P.E.P. In performing the obviousness inquiry under 35 U.S.C. §103, the Examiner must avoid hindsight. *In re Bond,* 910 F.2d 831, 834, 15 USPQ2d 1566, 1568 (Fed. Cir. 1990), *reh'g denied,* 1990 U.S. App. LEXIS 19971 (Fed. Cir. 1990).

II. Rejection of Claims 1-20 under 35 U.S.C. §103(a) as being unpatentable over Jenkins in view of Brickman

The Examiner has failed to set forth a case of *prima facie* obviousness under 35 U.S.C. §103(a) for claims 1-20. In particular, the Examiner has failed to demonstrate that the combination of Jenkins and Brickman teach or suggest all of the claim limitations of claims 1-20.

A. Rejection of Claims 1-8 and 15-20 under 35 U.S.C. §103(a) as being unpatentable over Jenkins in view of Brickman

Claim 1, as amended, recites, *inter alia*:

> a first expansion slot coupled to the first I/O controller; and
> a test module card directly coupled to the first expansion slot;
> wherein the test module card is configured to obtain access to a portion of the memory from the operating system, and wherein the test module card is configured to cause tests to be performed on the portion of the memory using direct memory access (DMA) subsequent to obtaining access to the portion of the memory.

Applicants respectfully submit that Jenkins and Brickman, either alone or in combination, do not teach or suggest all of the recited features of claim 1.

Jenkins does not teach or suggest "a test module card directly coupled to the first expansion slot" as recited in claim 1. The Office Action cites column 1, lines 30-32 of Jenkins as a teaching or suggestion of this feature of claim 1. At column 1, lines 27-32, Jenkins, in the "BACKGROUND OF THE INVENTION", teaches:

> One known factory tool is Compaq Diagnostics for DOS (disk operating system). This tool provides a suite of tests which can be run on the personal computer to test a variety of devices, such as memory, hard disks, floppy disks and serial ports. A specific module is provided to test each device.

This portion of Jenkins does not teach or suggest "a test module card directly coupled to the first expansion slot" as recited in claim 1. Instead, this portion of Jenkins appears to teach away from this feature of claim 1 by teaching that "the suite of tests ... can be run on the personal computer ... ." Col. 1, lines 28-29. This teaching of Jenkins implies that the suite of tests is executed by the processor of the personal computer rather than "a test module card directly coupled to the first expansion slot" as recited in claim 1.

Jenkins appears to teach a "hard disk drive 124" that contains a "diagnostic application 150" rather than a "test module card" as recited in claim 1. *See, e.g.,* column 3, line 67 to column 4, line 2 and Figure 1. Jenkins also teaches PCI slots 120 and ISA slots 138. *See* Figure 1. Jenkins does not teach or suggest that the diagnostic application 150 is

directly coupled to PCI slots 120 or ISA slots 138. Accordingly, Jenkins does not teach or suggest "a test module card directly coupled to the first expansion slot" as recited in claim 1.

In addition, Brickman does not teach or suggest "a first expansion slot coupled to the first I/O controller" or "a test module card directly coupled to the first expansion slot" as recited in claim 1. Brickman teaches a "port test card 300" that "can physically reside on any voice/data board 27 where it shares the common data transmit bus 44*a* and receive bus 44*b*". Column 59, lines 15-18. Brickman also teaches "[t]he test card further includes a direct memory access (DMA) control connected between a data output from the RAM and the transmit bus and connected between a data input to the RAM and the receive bus." Column 3, lines 1-5; *see also* column 59, lines 63-66. Brickman further teaches that "[a] voice port 20 or data port 14, 16, or 18 will be logically connected to the test card 300 via an intranodal connection through the intranodal buffer 56. These connections are controlled by entries into the switch control memory (SCM) 50." Column 59, lines 21-25. Because Brickman does not teach or suggest "a first expansion slot coupled to the first I/O controller" as recited in claim 1, Brickman does not teach or suggest "a test module card directly coupled to the first expansion slot" as recited in claim 1.

As described above, neither Jenkins nor Brickman teach or suggest "a test module card directly coupled to the first expansion slot" as recited in claim 1. Accordingly, Applicants respectively submit that claim 1 patentably distinguishes over Jenkins in view of Brickman for at least this reason.

Claim 1 further recites "wherein the test module card is configured to obtain access to a portion of the memory from the operating system, and wherein the test module card is configured to cause tests to be performed on the portion of the memory using direct memory access (DMA) subsequent to obtaining access to the portion of the memory." As noted in the Final Office Action mailed May 18, 2006 on page 6, Jenkins does not teach or suggest these features of claim 1. Brickman also does not teach or suggest these features of claim 1.

The Office Action cites "Col.2-3, lines 60-68 & 1-5" of Brickman as a teaching or suggestion of these features of claim 1. At column 2, lines 60 to column 3, line 5, Brickman teaches:

> The invention includes a test card which a has a read-only memory (ROM) for storing test patterns for each of the data rates R_i. The test card further includes a random access memory (RAM) having an input connected to the ROM, for storing one of the test patterns from the ROM. The test card further includes a processor having control outputs to the RAM and the ROM for controlling the transfer of one of the test patterns from the ROM to the RAM for the data rate R_j of the data port under test. The test card further includes a direct memory access (DMA) control connected between a data output from the RAM and the transmit bus and connected between a data input to the RAM and the receive bus.

This portion of Brickman does not teach or suggest the above features recited in claim 1. Instead, this portion of Brickman appears to teach away from these features of claim 1 by teaching that "the data port under test". Col. 3, line 1. Claim 1 recites that "the test module card is configured to cause tests to be performed on the portion of the memory", not a data port as taught by Brickman.

Other teachings of Brickman also teach away from these features of claim 1. At column 59, lines 11-14, Brickman teaches that "[t]here is one port test card 300 for the purpose of testing any SCC voice port 20 or data port 14, 16, or 18 and for testing certain portions of the digital switch 30." *See also* column 59, lines 33-37 and column 60, line 25 to column 61, line 15. Brickman also teaches that "the test port card includes ... a random access memory (RAM) 320, and a read-only memory (ROM) 318." Column 59, lines 38-42. Accordingly, Brickman does not teach or suggest "wherein the test module card is configured to obtain access to a portion of the memory from the operating system" or "wherein the test module card is configured to cause tests to be performed on the portion of the memory using direct memory access (DMA) subsequent to obtaining access to the portion of the memory" as recited in claim 1.

As described above, neither Jenkins nor Brickman teach or suggest the above features recited in claim 1. As a result, the Examiner has not set forth a case of *prima facie* obviousness under 35 U.S.C. §103(a) for claim 1. Applicants respectively submit that claim 1 patentably distinguishes over Jenkins in view of Brickman for at least these reasons.

Claims 2-8 depend from claim 1 and are believed to patentably distinguish over the cited references for at least the above reasons. Accordingly, Applicants respectfully request that the rejection of claims 1-8 under 35 U.S.C. §103(a) be withdrawn.

Applicants respectively submit the Examiner has not set forth a case of *prima facie* obviousness under 35 U.S.C. §103(a) for claim 15 for reasons similar to those given above from claim 1.

Claims 16-20 depend from claim 15 and are believed to patentably distinguish over the cited references for at least the above reasons. Accordingly, Applicants respectfully request that the rejection of claims 15-20 under 35 U.S.C. §103(a) be withdrawn.

B. Rejection of Claims 9-14 under 35 U.S.C. §103(a) as being unpatentable over Jenkins in view of Brickman

Claim 9 recites, *inter alia*:

> obtaining access to a portion of a memory of a computer system from an operating system during operation of a computer system;
>
> generating a test transaction in a test module card directly coupled to an expansion slot of the computer system; and
>
> providing the test transaction to the portion using direct memory access (DMA) subsequent to obtaining access to the portion of the memory.

Applicants respectfully submit that Jenkins and Brickman, either alone or in combination, do not teach or suggest all of the recited features of claim 9.

Jenkins does not teach or suggest "obtaining access to a portion of a memory of a computer system from an operating system during operation of a computer system" as recited in claim 9. Although the Examiner cites column 1, lines 28-31 of Jenkins as a teaching or suggestion of this feature (Final Office Action mailed May 18, 2006 at page 3), the Examiner also states that Jenkins "does not appear to explicitly disclose ... [that] the test module card is configured to obtain access to a portion of the memory from an operating system ... ." Final Office Action mailed May 18, 2006 at page 6.

At column 1, lines 28-31, Jenkins teaches that "[t]his tool provides a suite of tests which can be run on the personal computer to test a variety of devices, such as memory, hard

disks, floppy disks and serial ports." This portion of Jenkins does not teach or suggest "obtaining access to a portion of a memory of a computer system from an operating system during operation of a computer system" as recited in claim 9.

Although Brickman teaches a "port test card" as noted above with reference to claim 1, Brickman does not teach or suggest "obtaining access to a portion of a memory of a computer system from an operating system during operation of a computer system" as recited in claim 9.

As described above, neither Jenkins nor Brickman teach or suggest "obtaining access to a portion of a memory of a computer system from an operating system during operation of a computer system" as recited in claim 9. Accordingly, Applicants respectively submit that claim 9 patentably distinguishes over Jenkins in view of Brickman for at least this reason.

In addition, neither Jenkins nor Brickman teach or suggest "generating a test transaction in a test module card directly coupled to an expansion slot of the computer system" as recited in claim 9. The Examiner cites "308,310; figure 3" of Jenkins as a teaching or suggestion of this feature. Block 308 of Fig. 3 of Jenkins teaches "TEST LAUNCH", and Block 308 of Fig. 3 of Jenkins teaches "TEST EXECUTION". These teachings of Jenkins do not teach or suggest the above features of claim 9. Applicants respectfully submit that neither Jenkins nor Brickman teach or suggest these features of claim 9 for reasons similar to those given above with reference to claim 1. Accordingly, Applicants respectively submit that claim 9 patentably distinguishes over Jenkins in view of Brickman for at least this additional reason.

Further, neither Jenkins nor Brickman teach or suggest "providing the test transaction to the portion using direct memory access (DMA) subsequent to obtaining access to the portion of the memory" as recited in claim 9 As noted in the Final Office Action mailed May 18, 2006 on page 6, Jenkins does not teach or suggest these features of claim 9. Brickman also does not teach or suggest these features of claim 9 for reasons similar to those given above with reference to claim 1. Accordingly, Applicants respectively submit that claim 9 patentably distinguishes over Jenkins in view of Brickman for at least this further reason.

As described above, neither Jenkins nor Brickman teach or suggest the above features recited in claim 9. As a result, the Examiner has not set forth a case of *prima facie*

obviousness under 35 U.S.C. §103(a) for claim 9. Applicants respectively submit that claim 9 patentably distinguishes over Jenkins in view of Brickman for at least these reasons.

Claims 10-14 depend from claim 9 and are believed to patentably distinguish over the cited references for at least the above reasons. Accordingly, Applicants respectfully request that the rejection of claims 9-14 under 35 U.S.C. §103(a) be withdrawn.

C. Rejection of Claim 6 under 35 U.S.C. §103(a) as being unpatentable over Jenkins in view of Brickman

Dependent claim 6 recites "wherein the read and write transactions comprise DMA transactions". The Examiner cites column 3, line 56 of Jenkins as a teaching or suggestion of this feature of claim 6. At column 3, lines 55-57, Jenkins teaches that "[t]he PCI-to ISA bridge 122 integrates many of the common ISA peripherals, such as a DMA (Direct Memory Access) Controller ... ." This portion of Jenkins only identifies the existence of a DMA controller and does not teach or suggest "wherein the read and write transactions comprise DMA transactions" as recited in claim 6.

The Examiner also appears to cite "Brickman 306; figure 29" of Brickman as a teaching or suggestion of this feature of claim 6. Similar to the citation of Jenkins, this portion of Brickman only identifies the existence of a "direct memory access control (DMA)" 306 in FIG. 29 of Brickman and does not teach or suggest "wherein the read and write transactions comprise DMA transactions" as recited in claim 6.

Applicants respectively submit that claim 6 patentably distinguishes over the cited references for at least this additional reason. Accordingly, Applicants respectfully request that the rejection of claim 6 under 35 U.S.C. §103(a) be withdrawn for this additional reason.

D. Rejection of Claim 19 under 35 U.S.C. §103(a) as being unpatentable over Jenkins in view of Brickman

Dependent claim 19 recites "wherein the test module card is configured to cause tests to be performed on the memory using direct memory access (DMA)". The Office Action cites column 3, lines 55-57 of Jenkins as a teaching or suggestion of this feature of claim 19. At column 3, lines 55-57, Jenkins teaches that "[t]he PCI-to ISA bridge 122 integrates many of the common ISA peripherals, such as a DMA (Direct Memory Access) Controller ... ."

This portion of Jenkins only identifies the existence of a DMA controller and does not teach or suggest "wherein the test module card is configured to cause tests to be performed on the memory using direct memory access (DMA)" as recited in claim 19. Jenkins does not appear to teach or suggest that diagnostic application 150 is "is configured to cause tests to be performed on the memory using direct memory access (DMA)" as recited in claim 19. Brickman also does not teach or suggest this feature of claim 19.

Applicants respectively submit that claim 19 patentably distinguishes over the cited references for at least this additional reason. Accordingly, Applicants respectfully request that the rejection of claim 19 under 35 U.S.C. §103(a) be withdrawn for this additional reason.

CONCLUSION

For the above reasons, Appellants respectfully submit that the cited references neither anticipate nor render obvious the claims of the pending Application. The pending claims distinguish over the cited references, and therefore, Appellants respectfully submit that the rejections must be withdrawn, and respectfully request the Examiner be reversed and claims 1-20 be allowed.

Any inquiry regarding this Appeal Brief should be directed to either David Plettner at Telephone No. (408) 447-3013, Facsimile No. (408) 447-0854, or Christopher P. Kosh at Telephone No. (512) 241-2405, Facsimile No. (512) 241-2409. In addition, all correspondence should continue to be directed to the following address:

HEWLETT-PACKARD COMPANY
Intellectual Property Administration
P.O. Box 272400
Fort Collins, Colorado 80527-2400

Respectfully submitted,

Andrew H. Barr et al.

By their attorneys,

DICKE, BILLIG & CZAJA, PLLC
Fifth Street Towers, Suite 2250
100 South Fifth Street
Minneapolis, MN 55402
Telephone: (612) 573-2000
Facsimile: (612) 573-2005

Dated: 11-13-06

CPK:dmd

Christopher P. Kosh
Reg. No. 42,760

CERTIFICATE UNDER 37 C.F.R. 1.8:

The undersigned hereby certifies that this paper or papers, as described herein, are being deposited in the United States Postal Service, as first class mail, in an envelope address to: Mail Stop Appeal Brief – Patents, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on this 13th day of **November**, **2006**.

By_____
Name: Denyse Dauphinais

CLAIMS APPENDIX

1. (Previously Presented) A computer system comprising:

a processor configured to execute an operating system;

a memory controller coupled to the processor;

a memory coupled to the memory controller;

a first input/output (I/O) controller coupled to the memory controller;

a first expansion slot coupled to the first I/O controller; and

a test module card directly coupled to the first expansion slot;

wherein the test module card is configured to obtain access to a portion of the memory from the operating system, and wherein the test module card is configured to cause tests to be performed on the portion of the memory using direct memory access (DMA) subsequent to obtaining access to the portion of the memory.

2. (Previously Presented) The computer system of claim 1 wherein the processor is configured to cause the operating system to be booted, and wherein the test module card is configured to cause the tests to be performed on the portion of the memory subsequent to the operating system being booted.

3. (Previously Presented) The computer system of claim 1 wherein the test module card is configured to cause the tests to be performed on the portion of the memory during execution of the operating system.

4. (Original) The computer system of claim 1 further comprising:

a second I/O controller coupled to the memory controller;

a second expansion slot coupled to the second I/O controller; and

an I/O device coupled to the second expansion slot.

5. (Original) The computer system of claim 1 wherein the test module card is configured to cause tests to be performed on the memory by providing read and write transactions to the first I/O controller.

6. (Original) The computer system of claim 5 wherein the read and write transactions comprise DMA transactions.

7. (Original) The computer system of claim 1 further comprising:
a bus bridge coupled to the processor and the first I/O controller.

8. (Original) The computer system of claim 1 further comprising:
a system controller that comprises the memory controller.

9. (Previously Presented) A method comprising:
obtaining access to a portion of a memory of a computer system from an operating system during operation of a computer system;
generating a test transaction in a test module card directly coupled to an expansion slot of the computer system; and
providing the test transaction to the portion using direct memory access (DMA) subsequent to obtaining access to the portion of the memory.

10. (Original) The method of claim 9 further comprising:
detecting an error that occurs in response to the test transaction; and
performing a remedial action in response to detecting the error.

11. (Previously Presented) The method of claim 9 further comprising:
providing the test transaction from the test module to an I/O controller coupled to the expansion slot;
providing the test transaction from the I/O controller to a bus bridge;
providing the test transaction from the bus bridge to a system bus;
providing the test transaction from the system bus to a memory controller; and
providing the test transaction from the memory controller to the portion.

12. (Original) The method of claim 11 further comprising:

storing information in the memory in response to the test transaction being a write transaction.

13. (Original) The method of claim 11 further comprising:

in response to the test transaction being a read transaction:

providing information associated with the test transaction from the portion to the memory controller;

providing the information from the memory controller to the system bus;

providing the information from the system bus to the bus bridge;

providing the information from the bus bridge to the I/O controller; and

providing the information from the I/O controller to the test module.

14. (Previously Presented) The method of claim 9 further comprising:

providing the test transaction from the test module to an I/O controller coupled to the expansion slot;

providing the test transaction from the I/O controller to a system controller;

providing the test transaction from the system controller to a memory controller; and

providing the test transaction from the memory controller to the portion.

15. (Previously Presented) A computer system comprising:

a processor;

a memory controller coupled to the processor and configured to perform error correction;

a memory coupled to the memory controller;

an input/output (I/O) controller coupled to the memory controller;

an expansion slot coupled to the I/O controller; and

a test module card directly coupled to the expansion slot;

wherein the test module card is configured to obtain access to a portion of the memory from an operating system, and wherein the test module card is configured to cause tests to be performed on the portion of the memory by providing read transactions associated

with the memory to the I/O controller subsequent to obtaining access to the portion of the memory.

16. (Previously Presented) The computer system of claim 15 further comprising:

the operating system;

wherein the processor is configured to cause the operating system to be booted, and wherein the test module is configured to cause the tests to be performed on the memory using DMA subsequent to the operating system being booted.

17. (Previously Presented) The computer system of claim 15 further comprising:

the operating system;

wherein the processor is configured to cause the operating system to be executed, and wherein the test module is configured to cause the tests to be performed on the memory using DMA during execution of the operating system.

18. (Previously Presented) The computer system of claim 15 wherein the I/O controller provides the read transactions to a system bus.

19. (Previously Presented) The computer system of claim 15 wherein the test module card is configured to cause tests to be performed on the memory using direct memory access (DMA).

20. (Original) The computer system of claim 15 wherein the read transactions comprise direct memory access (DMA) transactions.

EVIDENCE APPENDIX

None.

RELATED PROCEEDINGS APPENDIX

None.